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APPLICATION NO	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO
09/433,705	11/04/1999	SHUNPEI YAMAZAKI	0756-2062	2883
22204	7590	10/08/2002	EXAMINER	
NIXON PEABODY, LLP 8180 GREENSBORO DRIVE SUITE 800 MCLEAN, VA 22102			LOKE, STEVEN HO YIN	
		ART UNIT	PAPER NUMBER	
		2811		

DATE MAILED: 10/08/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/433,705	YAMAZAKI, SHUNPEI
	Examiner	Art Unit
	Steven Loke	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 08 July 2002.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 13-45 is/are pending in the application.
- 4a) Of the above claim(s) 18-45 is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 13-17 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
 If approved, corrected drawings are required in reply to this Office action.
- 12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
 * See the attached detailed Office action for a list of the certified copies not received.
- 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
 a) The translation of the foreign language provisional application has been received.
- 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-1S2)
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>17,19,22</u> .	6) <input type="checkbox"/> Other: _____

1. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: The specification never discloses the second conductive layer can be made of an n-type silicon containing phosphorus and silicide as claimed in claim 16.

2. Claims 13 and 16 are objected to because of the following informalities: In claim 13, it is unclear whether "LDD" is being referred to "lightly doped drain". The phrase "LDD" should be in words instead of in abbreviation. In claim 16, line 3, there should be a "," after the phrase "(Ta)". Appropriate correction is required.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 13 and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakazono et al. (Japanese patent application no. 06-148685) in view of Kurokawa.

In regards to claim 13, Nakazono et al. disclose a semiconductor device in fig. 1. It comprises: a semiconductor island [2] on an insulating surface [1]; source and drain regions [7a] formed in the semiconductor island; a channel region [7c] in the semiconductor island between the source and drain regions; a pair of LDD regions [7b] formed between the channel region [7c] and the source and drain regions [7a]; a gate electrode [4, 5] formed over the semiconductor island with a gate insulating film [3] interposed therebetween wherein said gate electrode [4, 5] comprises at least a first

conductive layer [4] and a second conductive layer [5] formed on the first conductive layer [4].

Nakazono et al. differs from the claimed invention by not showing the first conductive layer having a pair of tapered portions, which extend beyond side edges of the second conductive layer. In addition, the pair of the LDD regions has a pair of first portions, which are overlapped by the pair of the tapered portions of the first conductive layer, and a pair of second portions, which extend beyond side edges of the first conductive layer.

Kurokawa shows a semiconductor device comprising a gate electrode [33] having a first conductive layer [31] having a pair of tapered portions, which extend beyond side edges of the second conductive layer [32] in fig. 2. In addition, a pair of the LDD regions [25] has a pair of first portions, which are overlapped by the pair of the tapered portions of the first conductive layer [31], and a pair of second portions, which extend beyond side edges of the first conductive layer [31].

Since both Nakazono et al. and Kurokawa teach an insulated gate electrode having two conductive layers and a pair of LDD regions, it would have been obvious to have the gate electrode structure and LDD regions of Kurokawa in Nakazono et al. because they prolong the life of the transistor and restrain the short channel effect.

In regards to claim 15, the combined device further discloses the semiconductor island is a crystalline silicon island.

In regards to claim 16, the combined device further discloses the first conductive layer includes an n-type silicon containing phosphorus and the second conductive layer includes tungsten silicide.

In regards to claim 17, Nakazono et al. and Kurokawa further differ from the claimed invention by not showing the devices as claimed in claim 17. It would have been obvious for the semiconductor device is one of the devices as claimed in claim 17 because they are widely used display devices that include a thin film transistor.

5. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakazono et al. in view of Kurokawa, further in view of Maddox, III.

Nakazono et al. and Kurokawa differ from the claimed invention by not showing the taper portion of the first conductive layer and the gate insulating film is in a range of 3 to 60 degrees.

Maddox, III discloses the taper portion of the gate electrode and the gate insulating film is less than 60 degrees in fig. 2.

Since both Kurokawa and Maddox, III teach an insulated gate transistor having a tapered gate electrode, it would have been obvious to have the tapered gate electrode of Maddox, III in Kurokawa because it minimizes the problem of punchthrough in the thin film transistor.

6. Applicant's remarks filed 7/8/02 have been fully considered but they are not persuasive.

The applicant said that he has no record of receiving acknowledgement of the Information Disclosure Statement filed on January 3, 2001. However, the Examiner never received an Information Disclosure Statement filed on January 3, 2001.

7. Applicant's arguments with respect to claims 13-17 have been considered but are moot in view of the new ground(s) of rejection.
8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (703) 308-4920. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers

for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

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October 6, 2002

Steven Loke